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3701 North Fairfax Drive
Arlington, VA 22203-1714

Attention: Mr. Douglas M. Pollock

Subject: Contract No. MDA972-93-C-0057; GTEL Project No. 852
Quarterly Technical Report (SLIN 0002AB)

Dear Mr. Pollock:

GTE Laboratories Incorporated hereby submits the subject report covering the period May 23, 1994 through August 23, 1994, in accordance with the terms of the Contract.

If you should have any questions or require any additional information or further clarification, please contact me at (617)466-2954.

Sincerely,

Deidre B. Ryan

Deidre B. Ryan
Contracts Manager

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Enclosure

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During the fourth quarter of the CORD Project substantial effort was devoted to refinement and interworking of the various system functions required to resolve network contentions optically. The system group at Stamford University continued the design and development of the CORD prototype and subsystems. This includes the subcarrier-multiplexing header transceiver, the pilot tone clock transceiver and the payload data transceiver. Substantial progress has also been made on the digital logic subsystems as well as the digital logic and analog/digital interface circuits for the 2.488 Gbps payload data channel.

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1. CONSORTIUM EXECUTIVE SUMMARY

During the fourth quarter of the CORD project, Stanford University continued the design and development of the CORD prototype and sub-systems. In particular, the 80 Mbps subcarrier-multiplexing header transceiver, the 2.488 GHz pilot tone clock transceiver, and the 2.488 Gbps payload data transceiver have been completed and characterized. A fully functional optical and microwave integrated transceiver, consisting of the three sub-system transceivers, has been implemented. The simultaneous transmission of payload data, clock tone, and header packets has been demonstrated. Our most recent efforts have been on the improvement of the system performance, which relies heavily on the filter design and power allocation for the three channels. An alternative filter solution has been investigated and is currently being developed to improve the overall system performance.

Substantial progress has also been made on the digital logic sub-systems. We have tested the header packet generation, transmission, and detection, logic circuitry with transmission through the microwave and optical sub-system. We have continued to refine our ultra-fast clock recovery technique, Delay-line Phase Alignment (DPA) and tested and characterized our prototype DPA circuit. The measured performance of the DPA prototype is sufficient for the CORD testbed and we expect substantial improvements in performance with the more integrated DPA circuit we are currently developing.

Also considerable progress was made in the digital logic and analog/digital interface circuits for the 2.488 Gbps payload data channel. Methods for byte synchronization of the demultiplexer and "start of ATM packet" detection have been developed. Design was completed of a hybrid CMOS, ECL, and GaAs circuit to multiplex and demultiplex data between 2.488 Gbps serial and 64-bit parallel, 39 MHz formats. Two interface circuits (DC-coupled and AC-coupled) between the analog payload data receiver and the digital logic have been investigated. We have selected an AC-coupled implementation with a limiting amplifier for the CORD testbed. Initial circuits have been built and the eye diagram and dynamic range of the limiting amplifier has been measured.

Our network-wide, slot synchronization technique has been further refined. Implemented was the slot delineator, or PING, detector with a digital oversampling technique, replacing the analog integrate and comparator circuit described in the previous progress report. This digital implementation is more immune to variations in received power levels and the additive noise from the receiving circuits.

Assembly of the CRO unit continued at GTE Laboratories. The lithium niobate switches from GEC Marconi were delivered at the end of July and required re characterization of the operating conditions. Integration of these switches with the delay lines, polarization monitors, and header detectors is in progress.

The semiconductor optical amplifier packages were fabricated and tested. The design requires a modification of the package for smooth operation of the course alignment mechanism. This work is in progress. In order to avoid additional delays associated with amplifier package refinement, a set of three amplifiers were ordered from HP, and delivery expected at the beginning of September.

Work on the semiconductor optical switch included a two dimensional modeling of the switch waveguide structure and fabrication of test structures for improved modal behavior of these devices. The modeling effort, being more accurate than our previous one, provided some guidance to the dimensional changes needed for single mode operation of the switch guide structure. These modifications are being implemented at the present time.

Also completed in this quarter was fabrication of polarization monitoring modules that permit a single polarization adjustment for proper CRO operation. These units were constructed and packaged and are being incorporated in the CRO module.

The main focus of UMass activity during the forth quarter has been the design of a simulator for (all-)optical networks, with particular attention being paid to optical devices and network functionalities required in the CORD project. The following tasks were completed: identification of two different layers for the simulator, defining the protocol specification layer and the ETS tool for Estelle protocol description purposes, defining the optical network specification layer.

At the present time there are several proposed all-optical network architectures and access protocols which take advantage of the most recent achievements in optical device designs. However, in most cases the research work on the access protocol and on the network architecture was completely done by one team, while the research work on optical devices was done independently by another team.

As a consequence, performance results obtained for many access protocols proposed for all-optical networks do not take in account the intricate specifics of the optical devices required to actually implement the respective network architectures. On the other hand, very detailed results obtained in studying and designing new optical devices are applied to very simplistic network architectures, mostly used for testbed demonstration, hence lacking of a global network view required in a practical solution.

For the above reason, one of the principal tasks of the CORD project at UMass is the development of a software package which will provide a solution to this problem by developing an integrated simulation tool for describing: a) the access protocol using Estelle formal description language, and b) the underlying all-optical network architecture, obtained by combining optical devices.

This ad-hoc developed software will allow the integration of the following operations: (optical) device characterization (loss, crosstalk, non linear effects, etc.) transmission system characterization (minimum SNR required, maximum dispersion allowed, maximum crosstalk allowed, etc.) network characterization (network architecture, access protocols, control strategies, routing strategies, etc.).

These three categories of information, which together constitute a comprehensive network description, will be integrated within the same simulation package to provide a modular and agile tool to evaluate performance in emerging all-optical network architectures. Impact on the network behavior resulting from changes occurring at any of the three levels of the system description will be made available to the user. For example, once a particular system is defined, one could evaluate the impact on system performance due to a specific parameter change, such as the change of power loss in a 2x2 switch, the change of modulation scheme, or the change of access protocol. The tool will also provide an integrated working environment where a device expert will be allowed to verify directly how his/her progress in a given optical component could affect the system behavior under analysis. Similarly, a network designer will be "forced" to work with a very detail characterization of the optical components, thus, dealing with situations that, very likely, represents real network conditions. To cope with the above objectives, the UMass research group has identified two different layers for the simulator tool, namely the protocol specification layer and the optical network specification layer.

As a base for the protocol specification layer we have selected ETS (Estelle Translator-Simulator). ETS is a CONSIP (Concurrent Network Simulator Package) based software tool which was designed and developed by the UMass research group. It allows one to develop layered protocols using the standard Estelle formal description language. Protocol entities can be modeled as concurrent processes running asynchronously. Due to its CONSIP platform, ETS provides a broad physical layer abstraction covering a variety of network topologies such as normal point-to-point networks, star, ring and other topologies. ETS also provides protocol description utilities, run time statistical results, and on-the-fly change of parameters for prompt evaluation of configuration changes. In order to "adapt" ETS for all-optical network specification and simulation, the necessary support has to be provided by the optical network specification layer. The all-optical physical layer, optical device libraries, all-optical network topology description utility, and new statistical functions will have to be supplemented by this simulator layer. The net result of this integration will be a flexible simulation tool for all-optical networks, which is derived from previous work (including code) completed at UMass for simulation of conventional networks.

The UMass team is currently working on the implementation of the simulator and its integration with the existing package ETS/CONSIP, and it is also moving its attention towards the important issue of CORD scalability, to provide large numbers of wavelengths in the system. Wavelength scalability is a critical aspect for the entire CORD project, and it will be carefully evaluated by considering the results obtained so far by the three participants of the consortium.

The following list provides a partial description of the main efforts for the next quarter at the UMass networking laboratory:

- Development of software code to provide the optical network simulator features described above.

- Preliminary investigation of alternative solutions to scale CORD approach to a large number of wavelengths (e.g., 8).

The section below contains the technical report of GTE Laboratories only. Stanford University and University of Massachusetts will submit their reports separately.

2. TECHNICAL SUMMARY

2.1 AMPLIFIER PACKAGING

An optical amplifier package similar to the design described in the last Quarterly Report was fabricated, assembled and tested. The package design incorporates both a course and fine fiber alignment mechanism to position the optical fiber with respect to the active amplifier chip. In testing the course-alignment adjustments we found that friction in the mechanism prevented smooth and repeatable motion of the fiber. Modifying the design to make it kinematic and using lubricants improved the mechanism action somewhat, but not enough to achieve the required alignment accuracy.

A new approach to course alignment is being developed which will require only slight modifications of the over-all amplifier package. Prototypes of this improved alignment hardware are currently being assembled and will be tested with optical amplifier chips which have been characterized and are ready for packaging.

2.2 POLARIZATION MONITORS

Polarization monitors were constructed similarly to the header detector using directional couplers and surface mounted photodetectors. The detector input includes a polarizer to reject the undesired polarization component. Therefore nulling out the photodetector output assures the proper polarization state at the input to the first optical switch. Use of polarization maintaining fibers in the CRO module assures that this polarization is maintained throughout the module. Two such units were fabricated and will be located at the two inputs past the demultiplexing stage. The figure below shows the fabricated device.

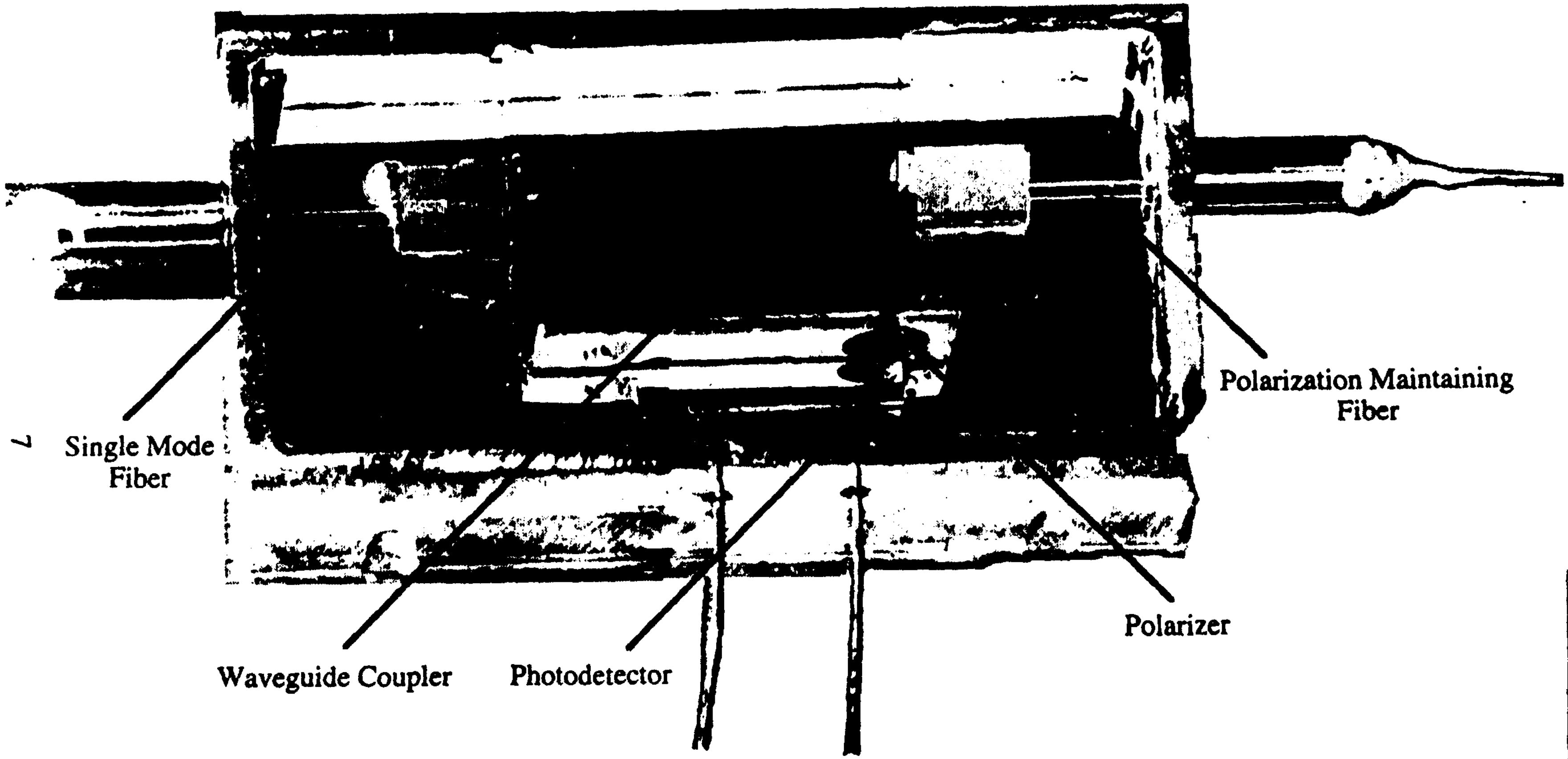

Fig. 1 Polarization Monitor

2.3 DIGITAL OPTICAL SWITCH

Last quarter we reported on a new plan of action to address the problem of higher-order spatial modes, which had limited the extinction ratio of the digital optical switches. In addition, the milestone for achieving a 2x2 switch was postponed to November 1994. This plan is now being carried out. The plan consists of three parts andthe results to date are as follows:

(a) Processing an epitaxial wafer which had previously yielded singlemode waveguides with 5 micron ridge widths.

A problem occurred during fabrication that resulted in shorting of the p-n junction, so that the switches were inoperable. The shorting cause has been identified and remedied by adjusting the polyimide thickness and etching times to ensure that polyimide covers the sides of the ridges. With this correction, fabrication has begun using two additional substrates from the same epitaxial wafer, and will be completed shortly.

(b) Fabricating an epitaxial wafer using a new mask which incorporates longer and curved waveguides, under the premise that these waveguides would strip out the higher-order spatial modes.

This step has been completed but structures not yet characterized, due to a one-month delay caused by the move and re-assembly of the characterization laboratory, as a result of ongoing building renovations. The new waveguide test mask uses ridge widths of 4.0, 4.5, and 5.0 microns for straight sections, and a ridge width of 5.0 microns for curved sections. The length of the curved section was varied (7, 14, 21, 28, and 35 degrees). This mask was used to fabricate waveguides using two wafers: one with quaternary and cladding layers of 0.35 micron, and one with quaternary and cladding layers of 0.40 micron, with other layers identical. The ridge height was about 2 microns. Initial results for the long, straight waveguides indicate that they are singlemode, due to the stripping effect of the longer length on higher order modes. (The fundamental mode loss was approximately 2.5 dB/cm.) These straight waveguides will be thoroughly characterized at their full length of 3.5 to 4.0 cm, and then shortened (by re-cleaving) and re-measured repeatedly until higher order modes appear.

(c) Identifying an improved epitaxial structure by the use of a two-dimensional modeling analysis.

Completed. Modeling results suggest that increasing the thickness of the InGaAs cap layer, and reducing the height of the ridge, will help in minimizing the higher order mode. On the basis of these results, four wafers have been ordered from EPI Products. These wafers will have the InGaAs cap layer increased from 0.1 micron to 0.15 micron, and the InP layer reduced from 2.0 microns to 1.0 microns. Two of the wafers will have a quaternary and cladding layer thickness of 0.40 microns, while the other two will have 0.35 microns.

Additional results from the modeling analysis, performed under contract at the University of Waterloo, include the correction of the refractive index due to material and waveguide dispersion in glass and semiconductor waveguides. These results will be used to extract the material indices from our experimental waveguide data for each new wafer.

In summary, the following will occur during the next quarter:

- The two already-completed waveguide test wafers will be fully characterized;

- Two switch wafers, fabricated from the same wafer as the waveguide tests, will be completed and characterized;

- Four new switch wafers, using the new design derived from modeling results, will be fabricated and tested.

- Modeling, which is temporarily on hold due to characterization delays arising from building renovation, will be resumed.

3 MILESTONES

In this quarter we planned to complete the construction of the preprototype CRO module and make it ready for the Stanford University group. The delay in availability of optical amplifiers will delay the completion of this milestone by about a month. We expect delivery of this device by mid September and completion of the milestone by the end of September.